IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	Kevin K. Main, et al.	
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Examiner	:	Cerullo, Jeremy	
Docket No.	:	TI-35983	
Customer No.	:	23494	
For	:	LPC TRANSACTION BRIDGING ACROSS A PCI_EXPRESS DOCKING CONNECTION	

AMENDMENT AFTER ALLOWANCE (37 C.F.R. § 1.312)

Commissioner of Patents
P. O. Box 1450
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Dear Sir:

In response to the examiner's amendments mailed February 28, 2006, applicants amend as follows.

Amendments to the Claims begin on page _2_ of this paper.

Remarks begin on page _6_ of this paper.

AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Previously Presented) A computer system comprising:

a portable computer having a LPC bus for peripheral devices;

a docking station receiving the portable computer and peripheral devices;

a PCI_Express (Revision 1.0a) fabric coupling the portable computer to the docking station, the PCI_Express (Revision 1.0a) fabric serial communicating commands or data between the LPC bus and the peripheral devices; and

a hybrid PCI_Express (Revision 1.0a) downstream port coupled to the LPC bus and to a computer host for receiving PCI_Express (Revision 1.0a) packets and LPC commands or data for transmission along PCI_Express (Revision 1.0a) fabric.

3. (Previously Presented) The computer system of Claim 2 further comprising a hybrid PCI_Express (Revision 1.0a) upstream port couplable to a peripheral device and receiving PCI_Express (Revision 1.0a) packets and LPC Transaction Packets from the PCI_Express (Revision 1.0a) fabric.

4. (Previously Presented) The computer system of Claim 2 wherein the hybrid PCI_Express (Revision 1.0a) downstream port receives a half-duplex LPC bus Transaction Packet and converts it to two full duplex PCI_Express (Revision 1.0a) packets for transmission on the PCI_Express (Revision 1.0a) fabric.

5. (Original) The computer system of Claim 4 further comprising a LPC packet manager which places a long wait sync clock signal on the LPC bus while awaiting a reply to a bi-directional LPC transaction data packet.

6. (Cancelled)

7. (Previously Presented) In a computer docking station to receive a portable computer and peripheral devices, a communications link between the portable computer and the peripheral devices comprising:

a PCI_Express (Revision 1.0a) fabric couplable to the portable computer and at least one of the peripheral devices, the PCI_Express (Revision 1.0a) fabric communicating commands or data between a computer in the docking station and a peripheral device connected thereto; and

a hybrid PCI_Express (Revision 1.0a) downstream port couplable to a LPC bus of a computer and to a computer host for receiving PCI_Express (Revision 1.0a) packets and LPC Transaction Packets for transmission along the PCI_Express (Revision 1.0a) fabric.

8. (Previously Presented) The computer docking station of Claim 7 further comprising a hybrid PCI_Express (Revision 1.0a) upstream port couplable to a peripheral device and receiving LPC Transaction Packets from the PCI_Express (Revision 1.0a) fabric.

9. (Previously Presented) The computer docking station of Claim 7 wherein the hybrid PCI_Express (Revision 1.0a) downstream port receives a half-duplex LPC bus Transaction packet and converts it to two full duplex PCI_Express (Revision 1.0a) packets for transmission on the PCI_Express (Revision 1.0a) fabric.

10. (Original) The computer docking station of Claim 9 further comprising a LPC packet manager which places a long wait sync clock signal on the LPC bus while awaiting a reply to a bi-directional LPC transaction data packet.

11. (Previously Presented) A modified PCI_Express (Revision 1.0a) fabric comprising:

a hybrid PCI_Express (Revision 1.0a) downstream port couplable to a computer LPC bus and to a computer host for receiving PCI_Express (Revision 1.0a) packets and LPC data or commands for transmission along PCI_Express (Revision 1.0a) fabric; and

a hybrid PCI_Express (Revision 1.0a) upstream port couplable to a computer peripheral device and receiving PCI_Express (Revision 1.0a) packets and packetized LPC data or commands from the PCI_Express (Revision 1.0a) fabric and separating out the LPC data or commands for use by the computer peripheral device.

12. (Currently Amended) The PCI_Express (Revision 1.0a) of Claim 11 further comprising a PCI_Express (Revision 1.0a) fabric coupled between the hybrid PCI_Express (Revision 1.0a) downstream port and the PCI_Express (Revision 1.0a) upstream port.

13. (Previously Presented) The PCI_Express (Revision 1.0a) fabric of Claim 11 wherein the hybrid PCI_Express (Revision 1.0a) downstream port receives a half-duplex LPC bus Transaction Packet and converts it to two full duplex PCI_Express (Revision 1.0a) packets for transmission on the PCI_Express (Revision 1.0a) fabric.

14. (Previously Presented) The PCI_Express (Revision 1.0a) of Claim 13 further comprising a LPC packet manager which places a long wait sync clock signal on the LPC bus while awaiting a reply to a bi-directional LPC transaction data packet.

15. (Previously Presented) A method of coupling LPC bus Transaction Packets across a boundary between a portable computer and a docking station utilizing a PCI_Express (Revision 1.0a) fabric comprising:

controlling the data flow on the PCI_Express (Revision 1.0a) fabric to insert at a first location on the PCI_Express (Revision 1.0a) fabric PCI_Express (Revision 1.0a) packets corresponding to LPC Transaction Packets into unused portions of the PCI_Express (Revision 1.0a) traffic,

receiving PCI_Express (Revision 1.0a) packets at a second location on the PCI_Express (Revision 1.0a) fabric and extracting those packets corresponding to the LPC Transaction Packets; and

performing an LPC task.

16. (Previously Presented) The method of Claim 15 further comprising converting half-duplex LPC bus Transaction Packets into two full duplex PCI_Express (Revision 1.0a) packets for transmission on the PCI_Express (Revision 1.0a) fabric.

17. (Previously Presented) In a method of coupling an LPC bus across a boundary between a portable computer and a docking station, a method of sending serial IRQ or DMA requests from a peripheral device to a processor, comprising:

generating in an LPC slave coupled to the peripheral device a PCI_Express (Revision 1.0a) upstream packet requesting a serial IRQ request or DMA request;

injecting the PCI_Express (Revision 1.0a) upstream packet into the PCI_Express (Revision 1.0a) fabric;

recovering the PCI_Express (Revision 1.0a) upstream packet in the docking station; and

utilizing the recovered PCI_Express (Revision 1.0a) upstream packet to generate sideband signals to an LPC controller.

18. (Original) The method of Claim 17 further comprising:

generating a serial IRQ or DMA request in the LPC controller.

REMARKS

The examiner's amendment inadvertently left out a word from Claim 12.

Respectfully submitted,
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